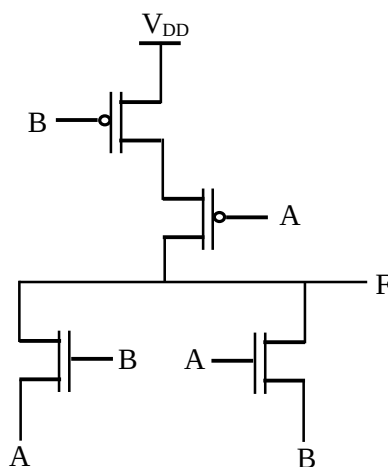


Digital Logic Families

ONE MARK QUESTIONS

- 4.1 When $V_{in} = 0$, $V_{out} = \text{High}$ and $V_{in} = 1$, $V_{out} = \text{Low}$. So, it is the voltage transfer characteristic of an inverter. If we closely inspect the slope of transition curve, it is very steep which is not observed in the case of BJT inverter. Therefore, it is the voltage transfer characteristic of a CMOS inverter i.e. option 'c'.
- 4.2 It is n-channel enhancement type of MOSFET. Therefore, both inputs must be high for output to be high which is nothing but AND gate. So, 'd' is the correct option.
- 4.3 Given circuit is similar to a 3-input inverter whose three inputs are A, B and $\bar{C}$.
 $\therefore Y = \overline{ABC} = \bar{A} + \bar{B} + C$ i.e. option 'a'.
- 4.4 We've studied these full forms in this chapter and the correct option is 'c'.
- 4.5 Redrawing the given schematic:



Here, expression for pull-up network is:

$$Y_p = \bar{A}\bar{B}$$

Similarly, expression for pull-down network is:

$$Y_d = AB + BA = AB$$

Therefore, final expression will be

$$F = \overline{Y_p} + Y_d = \overline{\bar{A}\bar{B}} + \bar{A}\bar{B} = \overline{\bar{A}\bar{B}}$$

$$\therefore F = (\bar{A} + \bar{B})(A + B) = \bar{A}B + A\bar{B}$$

which represents XOR operation i.e. option 'c'.

TWO MARK QUESTIONS

- 4.1 There exist two wired AND networks in the given circuit. One is at the output of XOR gate and the other is at the upper input terminal of the OR gate. So, the logic expression for Y is $Y = (\bar{X}_3(X_1 \oplus X_2)X_0)\bar{X}_0 + X_3$ which yields to $Y = X_3$ because due to $X_0\bar{X}_0$ the first term gets eliminated. Hence, the output will be high when is X_3 high which will be 8 times out of 16 possible combinations at the input.
- 4.2 When 2.5v is applied at the emitter of input Q_1 , it will be in the reverse active region. This will cause Q_2 to conduct and hence Q_2 will be in saturation region. As Q_2 is conducting, some potential drop will occur across $1k\Omega$ resistor which will forward bias the B-E junction of Q_3

and turn it ON. Therefore, Q_3 will conduct. We know that Q_3 and Q_4 act in push pull mode. Therefore, Q_4 will be in cut off region. It means 'b' is the correct option.

- 4.3** It is given that the output is at logic 0. So the transistor is in saturation and sink current i.e. $I_{sat} = 1 \text{ mA}$. It is also given that $V_{BE,sat} = 0.75$. This entails that the voltage drop across $1k\Omega$ resistor is $= 0.75$. Therefore, we can write $I_R = V_{BS,sat}/R = 0.75/1k\Omega = 0.75 \text{ mA}$. So, 'c' is the correct option.
- 4.4** We have studied in this chapter that DTL has low fanout, propagation delay is minimum in ECL and CMOS family has very low power consumption. So, 'b' is the correct option.
- 4.5** It is given that the diodes are ideal. So, there will be no voltage drop across them. If any input is held low that particular diode will get forward biased because anode is at 10V. This will pull down output node to logic low level. If all inputs are held high i.e. 10V is applied at the input terminals E_1 , E_2 and E_3 , the diodes will not conduct and output logic level will go high. This entails, it a 3-input AND gate which is option 'c'.